FREQUENCY GENERATION FOR A MULTI-BAND OFDM BASED ULTRA WIDE-BAND RADIO

The present invention relates to wideband RF communications systems, and more particularly to ultra-wideband (UWB) communications systems.

Ultra-Wideband Signals have been legal in the United States since February 2002 under conditions stipulated by the FCC Report and Order 02-48. Briefly, UWB signals must never be transmitted with a power spectral density of more than –41.2dBm/MHz in a band from 3.1GHz to 10.7GHz. Elsewhere, the power must be reduced even further to protect existing services. Since the power limit is specified as a power spectral density, the transmit power is proportional to the bandwidth, and hence the desire is to occupy as much bandwidth as possible within economic and feasibility constraints and thereby maximize the possible link range. However, due to the increasing RF path loss with carrier frequency, as well as increasing noise figure of semiconductor devices, initial interest is concentrated on exploiting the spectrum from 3.1 – 4.9GHz.

Two competing standards proposals for UWB have emerged, one identified with Motorola and the other identified with a coalition of companies referred to as the Multiband OFDM Alliance (MBOA). The MBOA-OFDM (hereinafter "MB-OFDM") system borrows heavily from the existing wireless LAN concepts for 802.11a and 802.11g. The OFDM signal consists of 128 sub-carriers. These carriers occupy a 528MHz, so the sub-carrier spacing is 4.125MHz. Since the carrier spacing is 4.125MHz, it follows that the OFDM symbol length must be 1/4.125e6 = 242.42 ns. To allow for inter-symbol interference a zero-energy prefix of ¼ of the symbol length (60.6 ns) is applied in place of the more traditional cyclic prefix. Finally a guard period of 5 samples (9.47ns) is added. The total OFDM symbol length is 312.5ns.

Of the 128 sub-carriers, 5 are set to nulls at the band edges, so that the actual occupied bandwidth is only 507.375MHz (marginally wider than the mandated 500MHz). Moreover, only 100 of the 128 sub-carriers are information-bearing; the others are either pilots, user-defined, or nulls. The 100 information-bearing tones carry QPSK modulation, thus providing 2 bits each, or 200 bits per OFDM symbol. The total gross information rate is thus (200/312.5e-9), or 640Mbps. After channel coding redundancy is taken into account, the maximum protected data rate is 480Mbps (3/4 rate code).

As noted above the plain use of OFDM results in an occupied spectrum of just over 500MHz, which is less than a third of the UWB spectrum available below 5GHz. Since the

transmitted power is proportional to the occupied bandwidth, failure to address this would have a serious impact on the available range. The MB-OFDM specification uses a 3-band hopping scheme to realize a 3-fold increase in bandwidth. The method adopted is that successive OFDM symbols are transmitted in different bands according to a predefined hopping sequence of length 6. These hopping sequences are designed to minimize collisions between uncoordinated piconets and are called Time- Frequency Interleaving (TFI) Codes. Example sequences include {1,2,3,1,2,3}, {3,2,1,3,2,1}, {1,1,2,2,3,3} etc., where each index represents a specific 528MHz frequency band.

The following table shows how PHY-SAP data rates from 53.3 to 480Mbps are derived from the basic 640Mbps uncoded bit rate, where redundancy is introduced by three mechanisms including convolutional coding (rate 1/3, 11/32, ½, 5/8 and ¾), conjugate symmetric input to the IFFT (introduces a factor of ½), and Time spreading, where complete OFDM symbols may be repeated on different frequencies.

Data Rate (Mb/s)	Modulation	Coding rate (R)	Conjugate Symmetric Input to IFFT	Time Spreading Factor (TSF)	Overall Spreading Gain	Coded bits per OFDM symbol (N_{CBPS})
53.3	QPSK	**1/3**	**Yes**	**2**	**4**	**100**
55	QPSK	**11/32**	**Yes**	**2**	**4**	**100**
80	QPSK	**½**	**Yes**	**2**	**4**	**100**
106.7	QPSK	**1/3**	**No**	**2**	**2**	**200**
110	QPSK	**11/32**	**No**	**2**	**2**	**200**
160	QPSK	**½**	**No**	**2**	**2**	**200**
200	QPSK	**5/8**	**No**	**2**	**2**	**200**
320	QPSK	**½**	**No**	**1 (No spreading)**	**1**	**200**
400	QPSK	**5/8**	**No**	**1 (No spreading)**	**1**	**200**
480	QPSK	**¾**	**No**	**1 (No spreading)**	**1**	**200**

Figure 1 shows the arrangement of sub-bands in the MB-OFDM UWB proposal. The sub-bands are divided into groups (group A, group B, group C and group D). An initial implementation contemplates the use of the three sub-bands of group A. A seven-band option has also been proposed, using the sub-bands of groups A and C. Sub-bands in groups B and D are presently reserved for possible future use.

Referring to Figure 2, a block diagram is shown of a known MB-OFDM UWB receiver frequency generator for generating the following three frequencies (in MHz): 3432, 3960 and 4488. (Unless otherwise noted, all frequency values set forth herein are given in MHz.) A PLL 201 coupled to a local oscillator 203 generates a frequency of 4224. This

signal is applied to two different paths 210 and 220. The first path connects the 4224 signal directly to one input of a single sideband (SSB) mixer 231. An output signal of the SSB mixer is the desired center frequency, i.e., either 3432, 3960 or 4488.

The second path includes a further SSB mixer 221, dividers 223 and 225, and a selector 227. The 4224 input signal is divided down successively by a factor of eight and again by two to produce a 264 signal applied to one input of the selector. The 264 signal is also applied to one input of the SSB mixer. The other input to the SSB mixer is a 528 signal obtained after the first divider 223. The SSB mixer outputs a 792 signal that is applied to the other input of the selector.

In the foregoing manner, the second path 220 generates frequencies of 264 and 792. One of the frequencies is selected by the selector 227 and applied to the second input of the SSB mixer 231 to generate the desired center frequency. In particular, when the second path generates the 264 signal, the SSB mixer outputs signals of 4224 ± 264, i.e., 4488 and 3960. Though not shown in this figure (or succeeding figures), the SSB mixer 231 generates both sum and difference ("+1 and –1") signals, and a gating circuit is used to select the desired center frequency. When the second path generates the 792 signal, the SSB mixer outputs signals of 4224 ± 792, i.e., 5016 (not used) and 3432.

SSB mixers, besides having considerable area and power requirements, typically produce output signals containing significant "spurs," i.e., unwanted frequency components. When multiple SSB mixers are connected in cascade as in Figure 2, the potential for unwanted spurs is greatly increased. Furthermore, because only a single desired frequency is generated at a time, system design requirements are imposed to ensure that the correct frequency is available and stable at the required time. Accordingly, a need exists for a frequency generator that overcomes the foregoing problems.

The present invention, generally speaking, provides for generation of at least three local oscillator signals for receiving a communication signal occupying corresponding sub-bands of a frequency band using one or more frequency synthesizers (e.g., PLLs or the like) and one or more single sideband mixers. In accordance with certain embodiments, only one single sideband mixer is encountered along the output path of a given local oscillator signal, thereby reducing spurs. In accordance with certain other embodiments, three local oscillator signals are generated continuously.

The present invention may be more fully understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is diagram showing the sub-band structure of the MB-OFDM UWB proposal;

Figure 2 is a block diagram of a known MB-OFDM UWB receiver frequency generator;

Figure 3 is a block diagram of a frequency generator in accordance with one embodiment of the present invention;

Figure 4 is a block diagram of another embodiment of a frequency generator;

Figure 5 is a block diagram of one variant of the frequency generator of Figure 4;

Figure 6 is a block diagram of another variant of the frequency generator of Figure 4;

Figure 7 is a block diagram of a further embodiment of a frequency generator;

Figure 8 is a table summarizing operation of the frequency generator of Figure 7;

Referring now to Figure 3, a block diagram is shown of a frequency generator according to one embodiment of the present invention. Two PLLs 310 and 320 are provided, driven by a common crystal oscillator XO. A first PLL includes a first VCO, VCO1, that receives a control signal 311 and produces identical output signals 313 and 315. A reference divider 317 divides down an output signal of the crystal oscillator and applies the resulting signal to a frequency/phase comparator 319. Similarly, an output divider 318 divides down an output signal of the crystal oscillator and applies the resulting signal to the frequency/phase comparator 319. The frequency/phase comparator 319 produces an error signal that is filtered by a loop filter 316 to produce the control signal 311. In the illustrated embodiment, the first PLL generates a frequency of 528, which is equal to the sub-band spacing.

The second PLL 320 is similar in its arrangement. In the illustrated embodiment, it generates a frequency of 3960, which is the center frequency of sub-band #2. Output signals of the first and second PLLs are mixed together in a SSB mixer 331 to generate frequencies of 3432 and 4488, corresponding to sub-bands #1 and #3, respectively.

Note that, in the foregoing embodiment and in other embodiments described hereafter, one or more of the VCOs may be run at some multiple of the frequencies shown with the relevant output signals being divided down. Such an arrangement may in some instances simplify the design of the VCOs. Furthermore, frequency synthesis techniques other than PLLs, such as direct digital synthesis (DDS) or delay lock loops (DLL) may be used

An alternative embodiment is illustrated in Figure 4. In this embodiment, PLL1 generates a frequency of 8976 and PLL2 generates a frequency of 6864. These frequencies are divided by two using dividers 401 and 403 to obtain frequencies of 4488 and 3432, corresponding to sub-band #3 and sub-band #1, respectively. Hence, in this embodiment, frequencies for two of the three sub-bands are generated directly, resulting in a reduction in spurs. One of the two frequencies generated directly is sub-band #3, which can entail the most demanding spur filtering requirements due to existing spectrum uses. By generating the frequency for sub-band #3 directly, filtering demands are reduced as compared to generating sub-band #3 using one or more SSB mixers (with resulting spurs).

The frequencies for sub-band #3 and sub-band #1 are again divided down by two (405, 407), and the resulting frequencies are mixed together in a SSB mixer 409 to obtain the frequency for sub-band #2 (4488/2 + 3432/2 = 7920/2 = 3960).

Variants of the clock generation circuit of Figure 4 are illustrated in Figures 5 and 6, respectively. The particular frequencies generated by the PLLs and the particular arrangement of the dividers may vary amongst a large number of possible arrangements, as illustrated by the exemplary embodiments of Figures 5 and 6.

Although the initial MB-OFDM proposal contemplates a three sub-band system using sub-bands #1-3, other systems may by extension use a different set of three sub-bands or may use a larger number of sub-bands. Four additional sub-bands available for use are sub-bands #6-9, for example, corresponding to frequencies of 6336, 6864, 7392, and 7920, respectively.

Referring to Figure 7, a clock generation circuit is shown capable of generating all of the foregoing frequencies. In the clock generation circuit of Figure 7, the frequencies generated by PLL1 and PLL2 are 7392 and 12672, respectively. The 7392 signal corresponds to sub-band #8 and is output directly. It is also input to a SSB mixer 701 for use in generating sub-bands #1-3, 6, 7 and 9. The 12672 signal is divided down by a programmable 1/K divider 703, where K may be 2, 3 or 6, followed by a ¼ divider 705. An output signal of the ¼ divider is input to the SSB mixer. The output signals generated by the SSB mixer include frequencies for sub-bands #6, 7 and 9. These latter frequencies are twice the respective frequencies of sub-bands #1, 2 and 3. Frequencies for sub-bands #1, 2 and 3 are therefore obtained by dividing by two (707) the output signal of the SSB mixer.

Figure 8 summarizes how the circuit of Figure 7 generates each of the frequencies involved, with the exception of sub-band #8, which is generated directly.

The foregoing clock generation circuits use two PLLs and one SSB mixer. Other clock generation circuits in accordance with other embodiments of the invention may use a greater or lesser number of PLLs and/or SSB mixers.

Referring to Figure 9, a clock generation circuit is shown that uses two PLLs 910 and 920 and two SSB mixers 931 and 933. The first PLL generates the frequency for sub-band #3 directly. The second PLL generates a frequency (1056) that is twice the sub-band spacing. This frequency is divided by two (935) to obtain a frequency (528) equal to the sub-band spacing.

The two SSB mixers are used to generate the frequencies for sub-bands #1and 2, respectively. To generate the frequency for sub-band #1, the 4488 signal is mixed with the 1056 signal. To generate the frequency for sub-band #1, the 4488 signal mixed with the 528 signal.

Referring to Figure 10, a clock generation circuit is shown that uses a single PLL 1010 and three SSB mixers 1011, 1013, and 1015. The PLL generates the frequency for sub-band #3 directly. The mixers 1011 and 1013 generate the frequencies for sub-bands #1 and 2, respectively, using as one input the frequency for sub-band #3. The other input is a frequency of 528 equal to the sub-band spacing (SSB mixer 1013) or a frequency of 1056 equal to twice the sub-band spacing (SSB mixer 1015). The latter frequencies are generated by a string of divide-by-two dividers 1017 and the SSB mixer 1015. The SSB mixer 1015 receives as inputs the frequency for sub-band #3 (4488) and the final output signal of the divider chain, which is a frequency of 264, and generates as an output signal a frequency of 4224. The divider chain produces intermediate frequencies of 2112, 1056 and 528.

In the embodiment of Figure 10, three local oscillator signals are generated continuously, simplifying system design.

It will be appreciated by those of ordinary skill in the art that the present invention may be embodied in other specific forms without departing from the spirit or essential character thereof. The present description is therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims and not the foregoing description, and all changes which come within the meaning and scope of equivalents thereof are intended to be embraced therein.